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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,812	06/26/2003	Kanakasabapathi Subramanian	1153.072US1	5482

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EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 10/606,812	Applicant(s) SUBRAMANIAN ET AL.	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.  
 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-39 is/are pending in the application.  
     4a) Of the above claim(s) 16, 23-30 and 33-39 is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-15, 17-22, 32 and 33 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/04 and 10/03</u> | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of group I invention, claims 1-15, 17-22 and 32-33 in the reply filed on February 14, 2005 is acknowledged.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-15, 17-22 and 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Milanovic et al., "Micromachining Technology for Lateral Field Emission Devices", IEEE Transactions on Electron Devices, Vol., 48, no. 1, January 2001, pp. 166-173.

Milanovic discloses a semiconductor process as claimed.

4. Pertaining to claim 1, Milanovic teaches a method of forming silicon wires in a single crystal silicon substrate, the method comprising; defining lines having a width; creating columns corresponding to the lines, the columns having ripples on both sides with a width comparable to the width of the lines; and oxidizing the columns to create silicon wires substantially corresponding to the ripples.

5. Pertaining to claim 2, Milanovic teaches the method of claim 1 wherein the width of the ripples is approximately equal to one-half the width of the lines.

Art Unit: 2823

6. Pertaining to claim 3, Milanovic teaches the method of claim 1 wherein the ripples are created by cyclically etching and passivating the columns.

7. Pertaining to claim 4, Milanovic teaches the method of claim 3 wherein the cycle time is between approximately 6 and 30 seconds.

8. Pertaining to claim 5, Milanovic teaches the method of claim 3 wherein etching comprises isotropic reactive ion etching.

Pertaining to claim 6, Milanovic teaches the method of claim 5 wherein SF<sub>6</sub> is used in the deep reactive ion etch.

9. Pertaining to claim 7, Milanovic teaches the method of claim 1 wherein the ripples are formed by a Bosch process.

10. Pertaining to claim 8, Milanovic teaches a method of forming nano-structures in a semiconductor substrate, the method comprising:

defining columns in the substrate;

repetitively etching and passivating sides of the column to create a column having ripples; and

oxidizing the ripples to form nano -structures.

11. Pertaining to claim 9, Milanovic teaches a method of creating a three dimensional array of wires in silicon substrate, the method comprising: defining an array of intersecting lines; creating columns corresponding to the lines, the columns having ripples on both sides with a width comparable to the width of the lines; and forming silicon wires substantially corresponding to the ripples, and extending between the columns defined by the support lines.

Art Unit: 2823

12. Pertaining to claim 10, Milanovic teaches the method of claim 9 wherein the width of lines and gap between lines is periodic in three dimensions for creating a photonic bandgap structure.

13. Pertaining to claim 11, Milanovic teaches the method of claim 9 wherein forming silicon wires comprises oxidizing, or aggressively etching the columns.

14. Pertaining to claim 12, Milanovic teaches a method of creating a three dimensional array of wires in silicon substrate, the method comprising: defining support pillars on the substrate, the pillars having a first width; defining wire lines on the substrate extending between the support pillars, and having a second width narrower than the first width; creating sidewalls corresponding to the support pillars and wire lines, the sidewalls having ripples on both sides with a width comparable to the width of the wire lines; and forming silicon wires substantially corresponding to the ripples, and extending between the pillars.

15. Pertaining to claim 13, Milanovic teaches the method of claim 12 wherein forming silicon wires comprises oxidizing, or aggressively etching the columns.

16. Pertaining to claim 14, Milanovic teaches a method of forming wires in a semiconductor substrate, the method comprising: defining a column; repetitively etching and polymerizing sides of the column to create a column having ripples; and oxidizing the column to form a wire surrounded by oxide.

17. Pertaining to claim 15, Milanovic teaches a method of forming wires in a semiconductor substrate, the method comprising:  
defining a column by use of a mask, wherein areas of the substrate adjacent the column comprise a floor;

Art Unit: 2823

repetitively etching the floor to create a column having rough sides;

passivating the etched column and floor between each etch;

clearing the floor of the substrate before each etch; and

oxidizing the column to form a wire surrounded by oxide.

18. Pertaining to claim 17, Milanovic teaches a method of creating a three dimensional array of nano-tips in a silicon substrate, the method comprising:

defining support lines on the substrate having a first width;

defining wire lines on the substrate extending between the support lines, and having a second width narrower than the first width;

creating columns corresponding to the support lines and wire lines, the columns having ripples on both sides with a width comparable to one-half the width of the wire lines; and oxidizing the columns to create silicon tips substantially corresponding to the ripples, and extending partially between the columns defined by the support lines.

19. Pertaining to claim 18, Milanovic teaches the method of claim 17 and further comprising removing oxide to expose the silicon nano-tips.

Pertaining to claim 19, Milanovic teaches a method of forming channels in a semiconductor substrate, the method comprising: defining a trench having two sides; repetitively etching and passivating the sides of the trench to create rough sides; and oxidizing the trench to form a channel surrounded by oxide.

20. Pertaining to claim 20, Milanovic teaches a method of forming channels in a semiconductor substrate, the method comprising: defining two side walls by use of a mask, wherein areas of the substrate adjacent the side walls comprise a floor;

Art Unit: 2823

repetitively etching the floor to create side walls having rough sides; polymerizing the etched sidewalls and floor between each etch; clearing the floor of the substrate before each etch; and oxidizing the side walls to form a channel between the sidewalls corresponding to at least one of the etches.

21. Pertaining to claim 21, Milanovic teaches a method of forming a sieve from a semiconductor substrate, the method comprising: defining multiple columns in the substrate; repetitively etching and passivating the columns to form ripples on the columns; etching the rippled columns to form wires substantially corresponding to the ripples; and oxidizing the wires to reduce spacing between the wires.

22. Pertaining to claim 22, Milanovic teaches the method of claim 21 wherein the columns are defined with a decreasing line spacing, resulting in a progressively reduced spacing between the wires.

23. Pertaining to claim 31, Milanovic teaches a method of creating a displacement sensor supported by a substrate, the method comprising:  
defining a column by use of a mask, the column comprising thicker support structures on both ends, wherein areas of the substrate adjacent the column comprise a floor;  
repetitively etching the floor to create a column having rough sides;  
passivating the etched column and floor between each etch;  
clearing the floor of the substrate before each etch; and oxidizing the column to form a wire surrounded by oxide which is thicker on both ends, and fully oxidized in the middle to form opposed tips a desired distance apart and supported by the support structures.

Art Unit: 2823

24. Pertaining to claim 32, Milanovic teaches the method of claim 31 wherein the distance is controlled to ensure that tunneling current via quantum effect is modified by slight displacements of the support structures.

*Conclusion*

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856.

The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman  
Primary Examiner  
Art Unit 2823